MADE EASY PUBLICATIONS

POSTAL BOOK PACKAGE 2025

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ELECTRONICS ENGINEERING

Objective Practice Sets

Analog Circuits

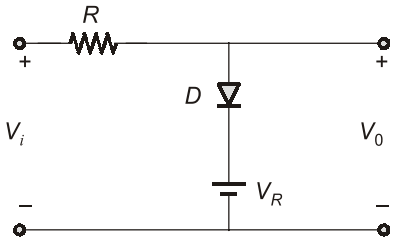
1 CHAPTER
Diode Circuit and Power Supply

MCQ and NAT Questions

Q.1 The voltage across diode at temperature T_1 is 0.76 V. If temperature is increased by 20°C at constant current the new voltage across diode is
(a) 0.65 V (b) 0.81 V
(c) 0.71 V (d) 0.7 V

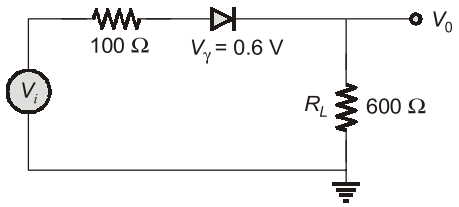
Q.2 A diode whose terminal characteristics are related as $i_D = I_s e^{V/V_T}$, where I_s is the reverse saturation current and V_T is thermal voltage (V_T = 25 mV), is biased at I_D = 4 mA. Its dynamic resistance is
(a) 12.5 Ω (b) 50 Ω
(c) 6.25 Ω (d) 25 Ω

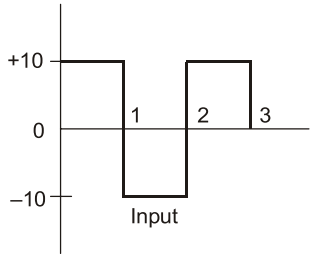
Q.3 In the circuit shown below the input V_i has positive and negative swings. V_o is the output.



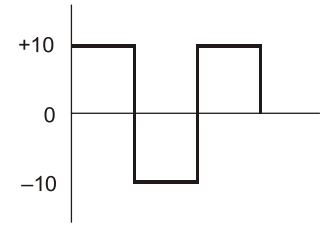
(a) V_o = 0 for negative V_i
(b) $V_o = V_R$ for positive V_i
(c) $V_o = V_R$ for $V_i > V_R$
(d) $V_o = V_R$ for all V_i

Q.4



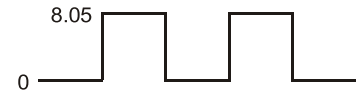


The output waveform is

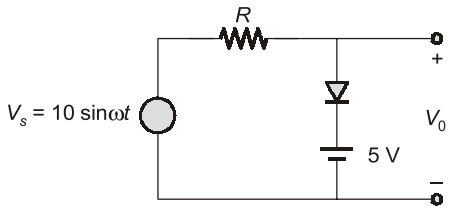
(a)


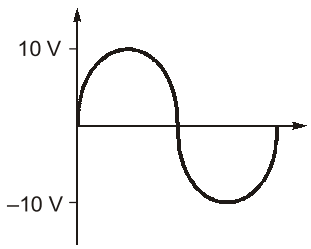
(b)

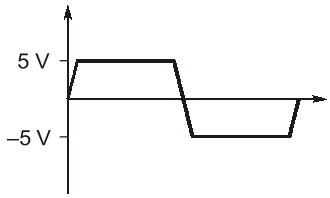

(c)

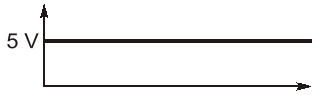

(d)


Q.5 For the circuit shown below assuming ideal diode, the output waveform V_0 is

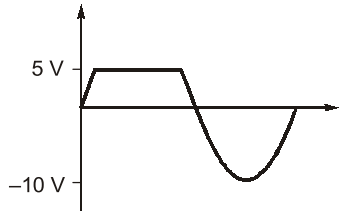


(a)


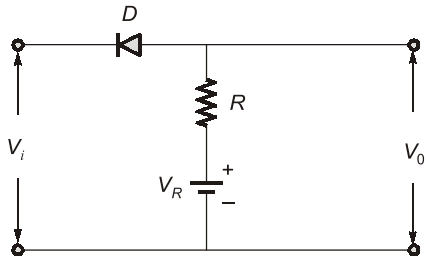
(b)


(c)


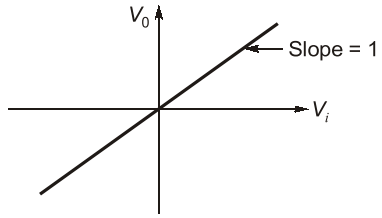
(d)



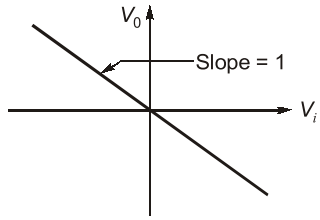
Q.6 The transfer characteristic of the network shown below is represented as



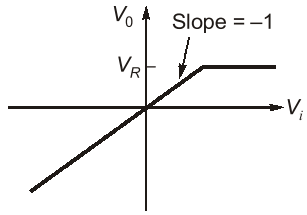
(a)



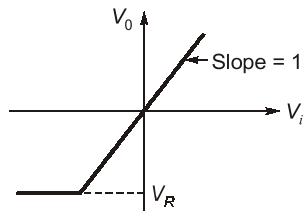
(b)



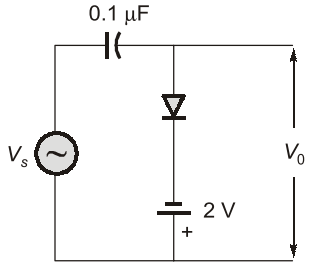
(c)



(d)

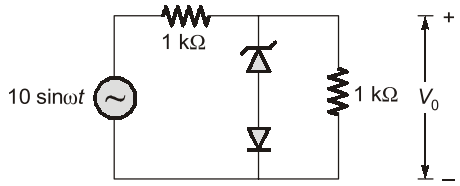


Q.7 For an input of $V_s = 5 \sin\omega t$, (assuming ideal diode), circuit shown below will behave as a



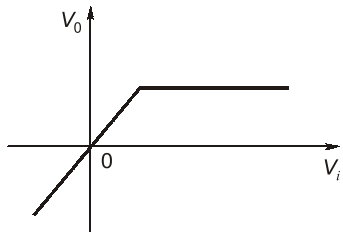
(a) clipper, sine wave clipped at –2 V
(b) clamper, sine wave clamped at –2 V
(c) clamper, sine wave clamped at zero volt
(d) clipper, sine wave clipped at 2 V

Q.8 The cut-in voltage of diode *D* shown in figure is 0.65 V, while breakdown voltage of the Zener Diode is 3 V. Diode is considered to be ideal. The value of peak output voltage V_o.



(a) 3 V in the positive half cycle and 0.65 V in the negative half cycle.
(b) 3.65 V in the positive half cycle and –5 V in the negative half cycle.
(c) 3 V in positive half cycle and –5 V in the negative half cycle
(d) –3.65 V in positive half cycle and 5 V in the negative half cycle

Q.9 The voltage transfer characteristic as shown in the figure will relate to a

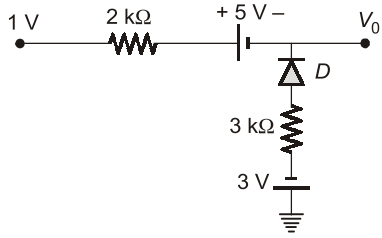


1. voltage regulator
2. half-wave rectifier
3. full-wave rectifier

Which of the above is/are correct?

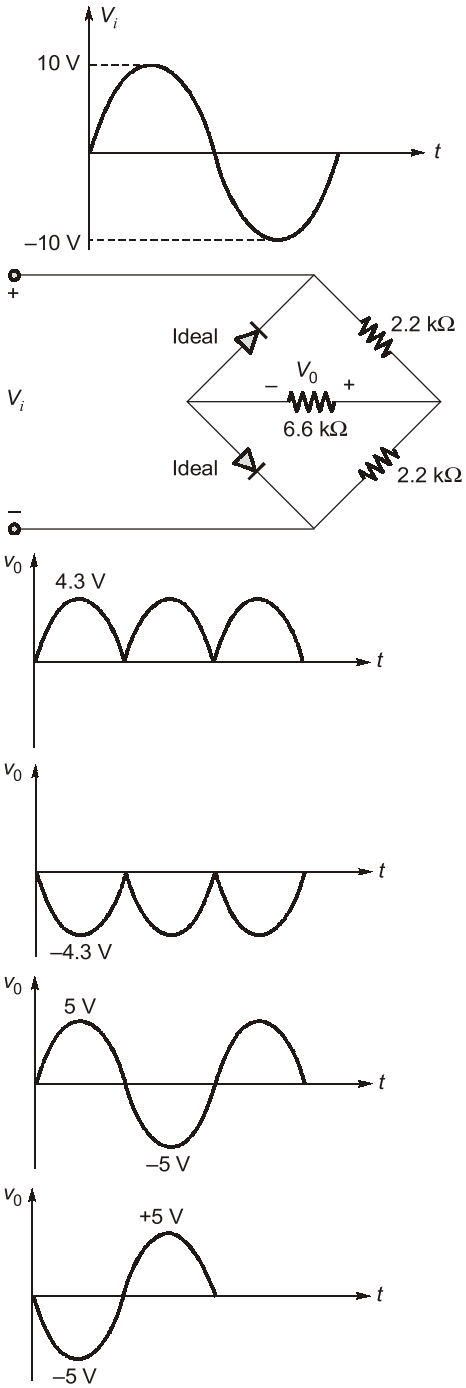
(a) 1 only (b) 2 only
(c) 1 and 2 (d) 1 and 3

Q.10 What is the output voltage V_0 for the circuit shown below assuming an ideal diode?

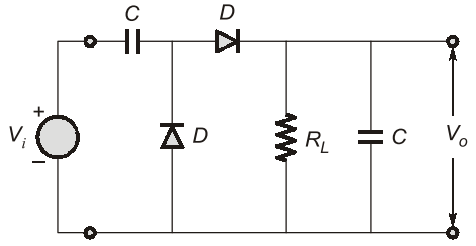


(a) $-\frac{18}{5}$ V (b) $\frac{18}{5}$ V
(c) $-\frac{13}{5}$ V (d) $\frac{13}{5}$ V

Q.11 The correct waveform for output (V_0) for below network is

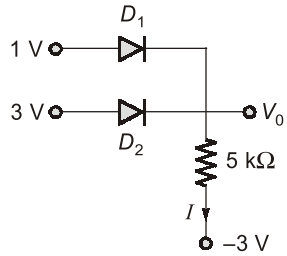


Q.12 Consider the below circuit, for $V_i = V_m \sin \omega t$, the output voltage V_o for $R_L \to \infty$ will be



(a) Zero (b) V_m
(c) $2V_m$ (d) $-V_m$

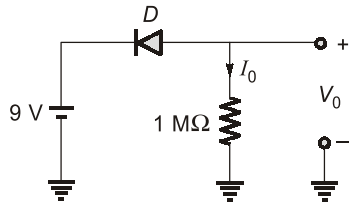
Q.13 Consider the circuit shown in the figure below



If diode D_1 and D_2 are made up of same material with the cut-in voltage $V_\gamma = 0.7$ V, then the value of current I is equal to

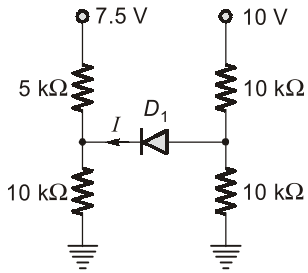
(a) 0.46 mA (b) 0.99 mA
(c) 0.59 mA (d) 1.06 mA

Q.14 Consider the diode circuit shown in the figure below:



The diode in the circuit is a large high-current silicon device whose reverse leakage current is reasonably independent of voltage appearing on the diode. If $V_0 = 1$ V at 20° C, then the value of output voltage at 40°C is equal to _____ V.

Q.15 Consider the circuit shown in the figure below



If the cut-in voltage of the diode D_1 is equal to 0.7 V, then the value of current flowing through the diode is equal to _____ mA.

Q.16 A 700 mW maximum power dissipation diode at 25°C has 5 mW/°C de-rating factor. If the forward voltage drop remains constant at 0.7 V, the maximum forward current at 65°C is

(a) 700 mA (b) 714 mA
(c) 1 A (d) 1 mA

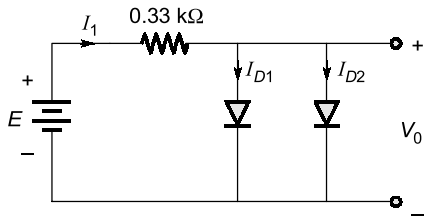
Q.35 A full wave rectifier delivers DC power of 50 W to a load of 200 Ω. If the ripple factor is 1%, the AC ripple voltage across the load is

(a) $\frac{1}{2}$ V (b) 1 V

(c) $\frac{2}{3}$ V (d) $\frac{3}{2}$ V

Multiple Select Questions (MSQs)

Q.36 For the circuit shown below :



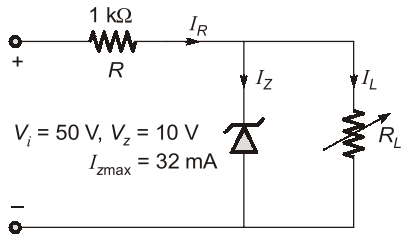
(where $E = 10$ V)

Which of the following statement is correct?

(a) $I_1 > I_{D1} > I_{D2}$ (b) $I_{D1} < I_{D2} < I_1$

(c) $I_{D1} = I_{D2} = \frac{I_1}{2}$ (d) $I_1 = 28.18$ mA

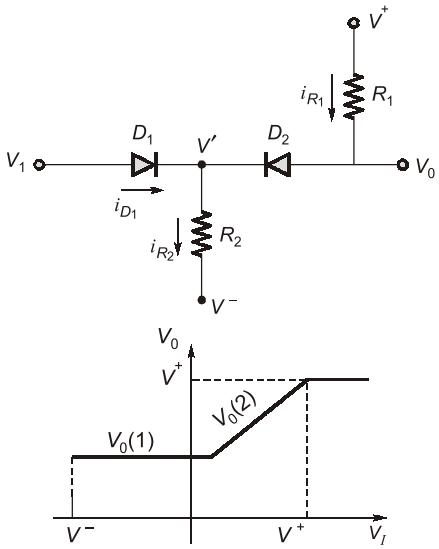
Q.37 For the network shown below, which of the following option(s) is/are correct regarding the range of R_L and I_L that will result in V_{R_L} being maintained at 10 V.



(a) $R_{L\,min} = 250\ \Omega$ (b) $I_{L\,min} = 8$ mA

(c) $R_{L\,max} = 1.25$ kΩ (d) $I_R = 40$ mA

Q.38 For the circuit shown below :



Assume the circuit parameters are $R_1 = 5$ kΩ, $R_2 = 10$ kΩ, $V_\gamma = 0.7$ V, $V^+ = +5$ V and $V^- = -5$V

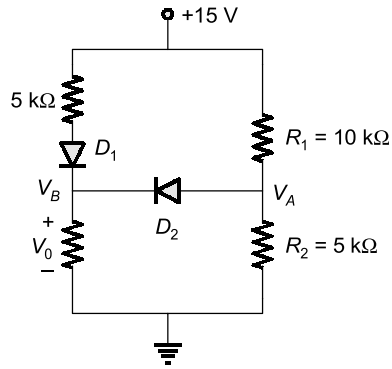
(a) For $V_1 = 0$, $i_{R1} = 0.62$ mA

(b) For $V_1 = 4$ V, $i_{R1} = 0.2$ mA

(c) For $V_1 = 4$ V, $i_{R2} = 0.83$ mA

(d) For $V_1 = 4$ V, $i_{D1} = 0.63$ mA

Q.39 For the circuit shown below :



Which of the following are correct?

(a) $V_A = 7.62$ V (b) $V_B = 6.92$ V

(c) $V_A = 5$ V (d) $V_B = 9.53$ V

Answers — Diode Circuit and Power Supply

1.	(c)	2.	(c)	3.	(c)	4.	(d)	5.	(d)	6.	(c)	7.	(b)
8.	(b)	9.	(a)	10.	(a)	11.	(a)	12.	(c)	13.	(d)	14.	(4)
15.	(0)	16.	(b)	17.	(a)	18.	(a)	19.	(c)	20.	(c)	21.	(a)
22.	(b)	23.	(b)	24.	(b)	25.	(a)	26.	(d)	27.	(c)	28.	(a)
29.	(c)	30.	(c)	31.	(d)	32.	(c)	33.	(d)	34.	(c)	35.	(b)
36.	(c, d)	37.	(a, b, c, d)	38.	(a, b, c, d)	39.	(c , d)						

Explanations **Diode Circuit and Power Supply**

1. (c)

$$\frac{dV_D}{dT} = -2.5\ \text{mV/°C}$$

$$\Delta V_D = 20 \times (-2.5\ \text{mV}) = -0.05\ \text{V}$$

$$\therefore \quad V_D + \Delta V_D = V_2 = 0.71\ \text{V}$$

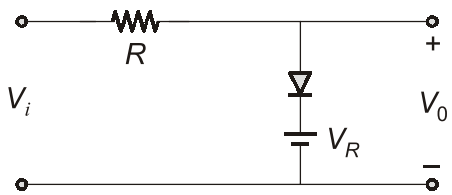
2. (c)

$$\frac{1}{r_d} = \frac{\partial I_D}{\partial V} = \frac{I_D}{V_T}$$

r_d : dynamic resistance.

$$\therefore \quad r_d = \frac{V_T}{I_D} = \frac{25}{4} = 6.25\ \Omega$$

3. (c)



Considering ideal diode :

for $V_i < V_R$, diode is OFF hence there is no current through R and $V_0 = V_i$.

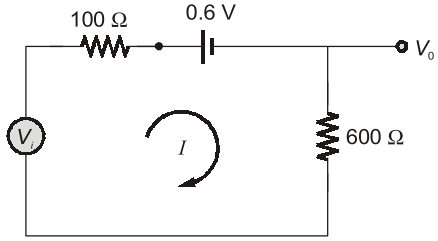
For $V_i > V_R$, diode is ON hence

$$V_0 = V_R$$

(as diode will act as short circuit)

4. (d)

For $0 \le t \le 1$, diode is ON



$$I = \frac{V_i - 0.6}{100 + 600} = \frac{10 - 0.6}{700}$$

$$= 0.01343\ \text{A}$$

$$\therefore \quad V_0 = 600 \times 0.01343 = 8.058\ \text{V}$$

for $1 < t < 2$, diode is OFF, there will be no current in the circuit and hence

$$V_0 = 0\ \text{V}$$

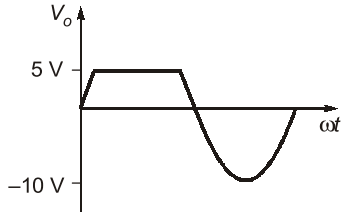
Hence output waveform can be given as shown below:

5. (d)

For $0 \le V_i < V_R$ = diode is OFF $\Rightarrow V_0 = V_i$

For $V_R \le V_i \Rightarrow$ diode is ON $\Rightarrow V_0 = 5$ V

Hence output waveform can be as shown below

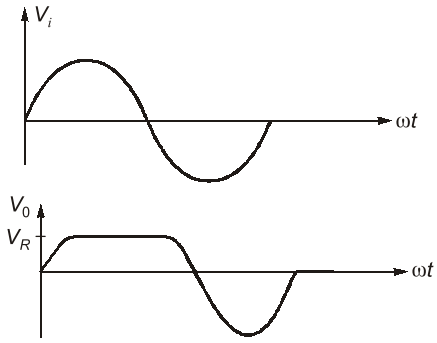


6. (c)

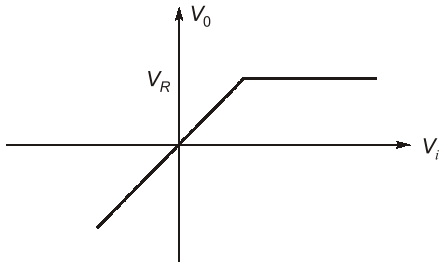
For $V_i < V_R$ = Diode is OFF $\Rightarrow V_0 = V_i$

For $V_i > V_R$ = Diode is ON $\Rightarrow V_0 \simeq V_R$

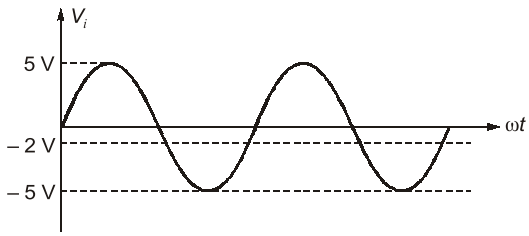
Hence for a sinusoidal input, output can be shown as below



Hence characteristic can be as shown below



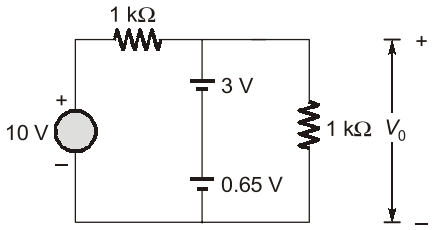
7. (b)



Hence given circuit acts as a clamper, sine wave clamped at – 2 V.

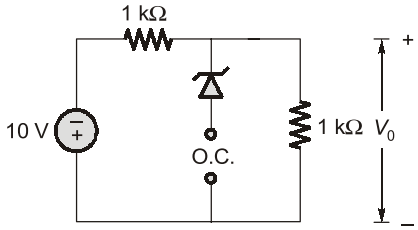
8. (b)

For positive half cycle:



So, $V_o = 3.65$ V

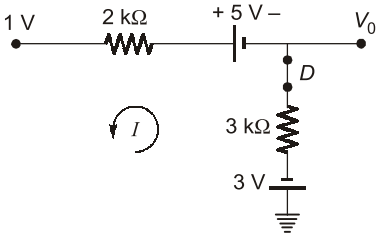
In negative half cycle:



So, $V_o = -5$ V

10. (a)

∵ Diode is forward bias (short circuit)



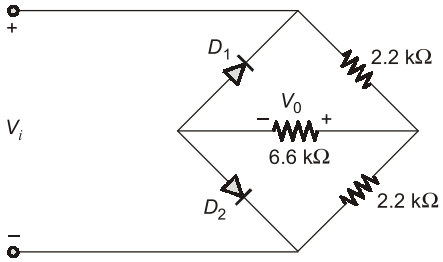
By applying KVL,

$3\text{ V} + 3\text{ k}\Omega I - 5\text{ V} + 2\text{ k}\Omega\, I + 1\text{ V} = 0$

$$I = \frac{1\text{V}}{5\text{k}\Omega} = \frac{1}{5}\text{ mA}$$

$$\therefore \quad V_o = -3 - 3\times\frac{1}{5} = -\frac{18}{5}\text{ V}$$

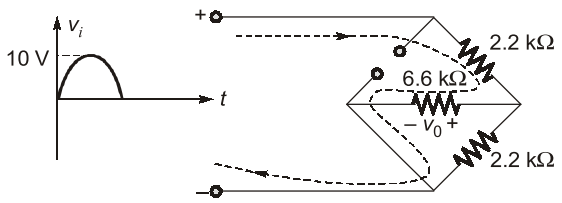
11. (a)



For positive half cycle of input voltage

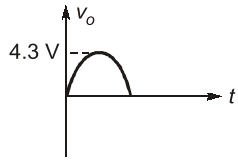
$D_1 \rightarrow$ OFF

$D_2 \rightarrow$ ON

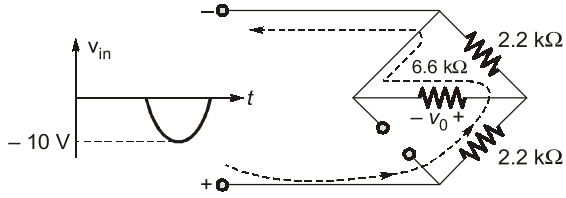


$$V_{o_{max}} = \frac{[6.6\,\text{k}\Omega \,\|\, 2.2\,\text{k}\Omega]}{2.2\,\text{k}\Omega + [6.6\,\text{k}\Omega \,\|\, 2.2\,\text{k}\Omega]} V_{i\,max}$$

$$= \frac{0.75}{1+0.75}\times 10\text{ V} = 4.3\text{ V}$$

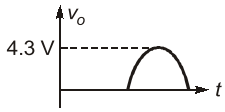


For negative half cycle of input voltage

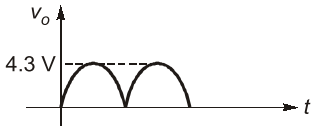


$$V_{o_{max}} = \frac{[6.6\,\text{k}\Omega \,\|\, 2.2\,\text{k}\Omega]}{2.2\,\text{k}\Omega + [6.6\,\text{k}\Omega \,\|\, 2.2\,\text{k}\Omega]} V_{i\,max}$$

$$= \frac{0.75}{1+0.75}\times 10\text{ V} = 4.3\text{ V}$$



Still the polarity of output voltage is in the same direction. So, net output of the circuit will be a full rectified wave.



12. (c)

The given circuit is a voltage doubler. Hence,

$$V_o = 2\,V_m$$

13. (d)

When D_2 is ON then the value of V_0 will be

$$V_0 = 3 - 0.7\text{ V} = 2.3\text{ V}$$

Hence, D_1 will be OFF.